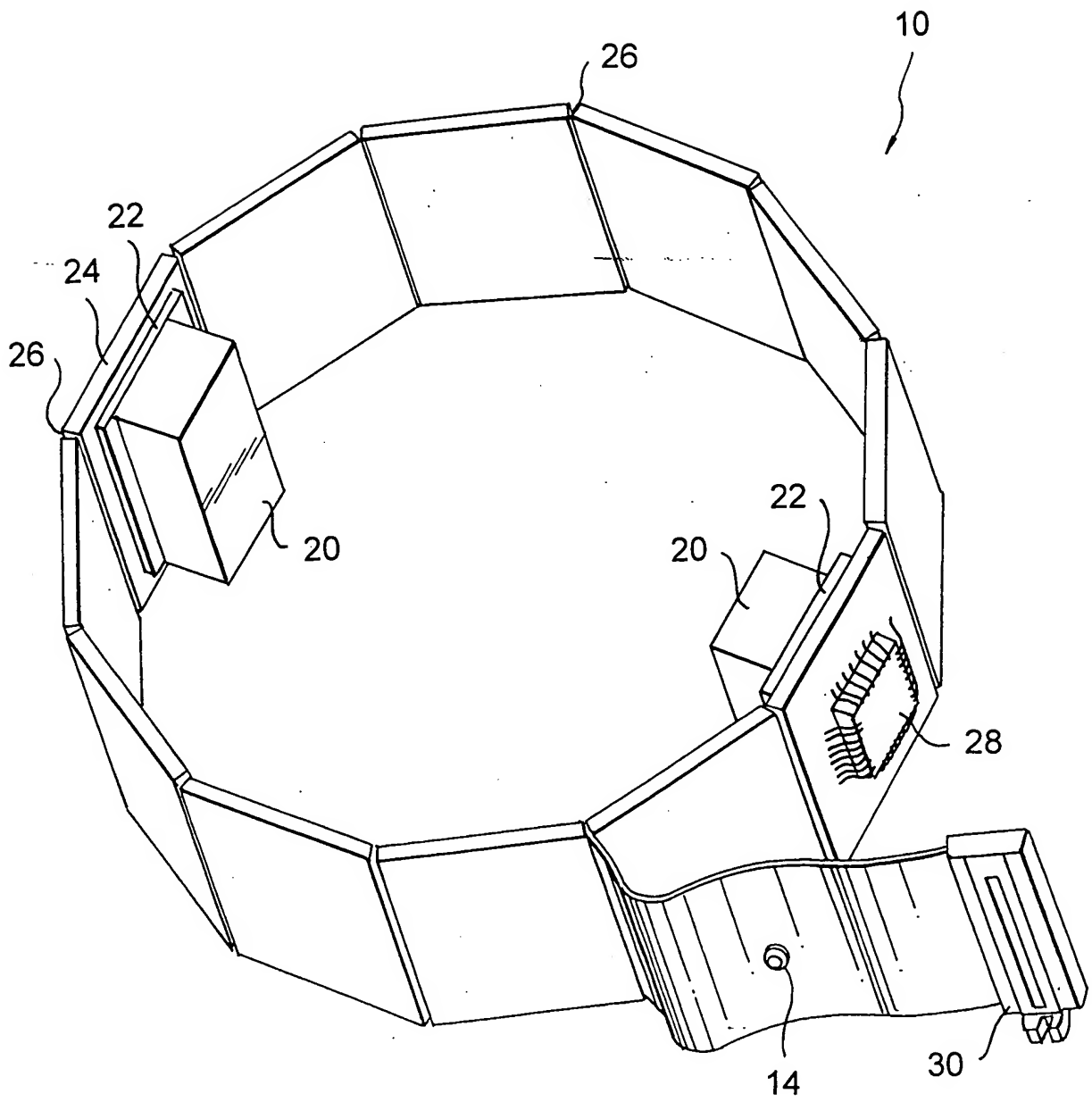
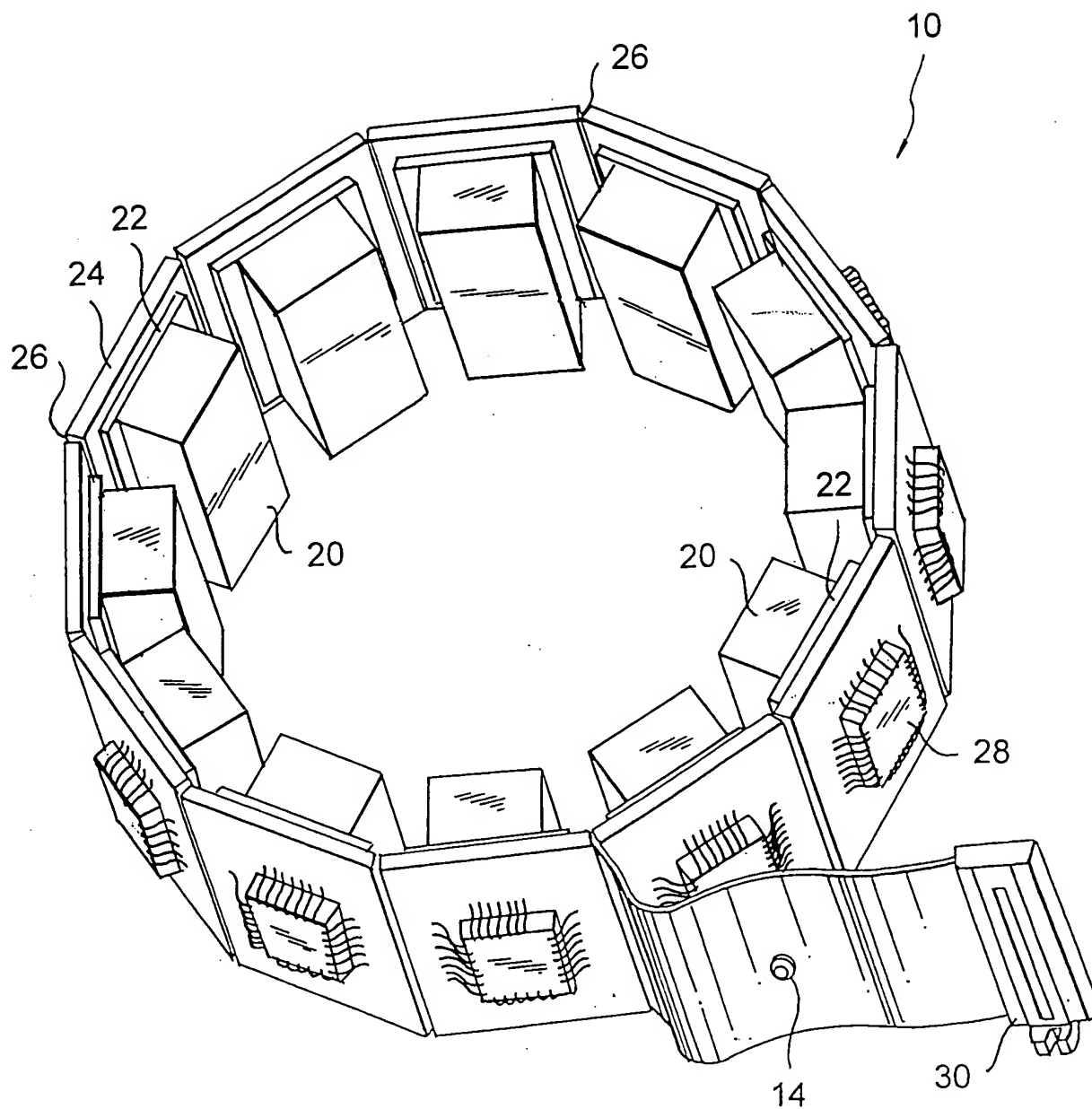


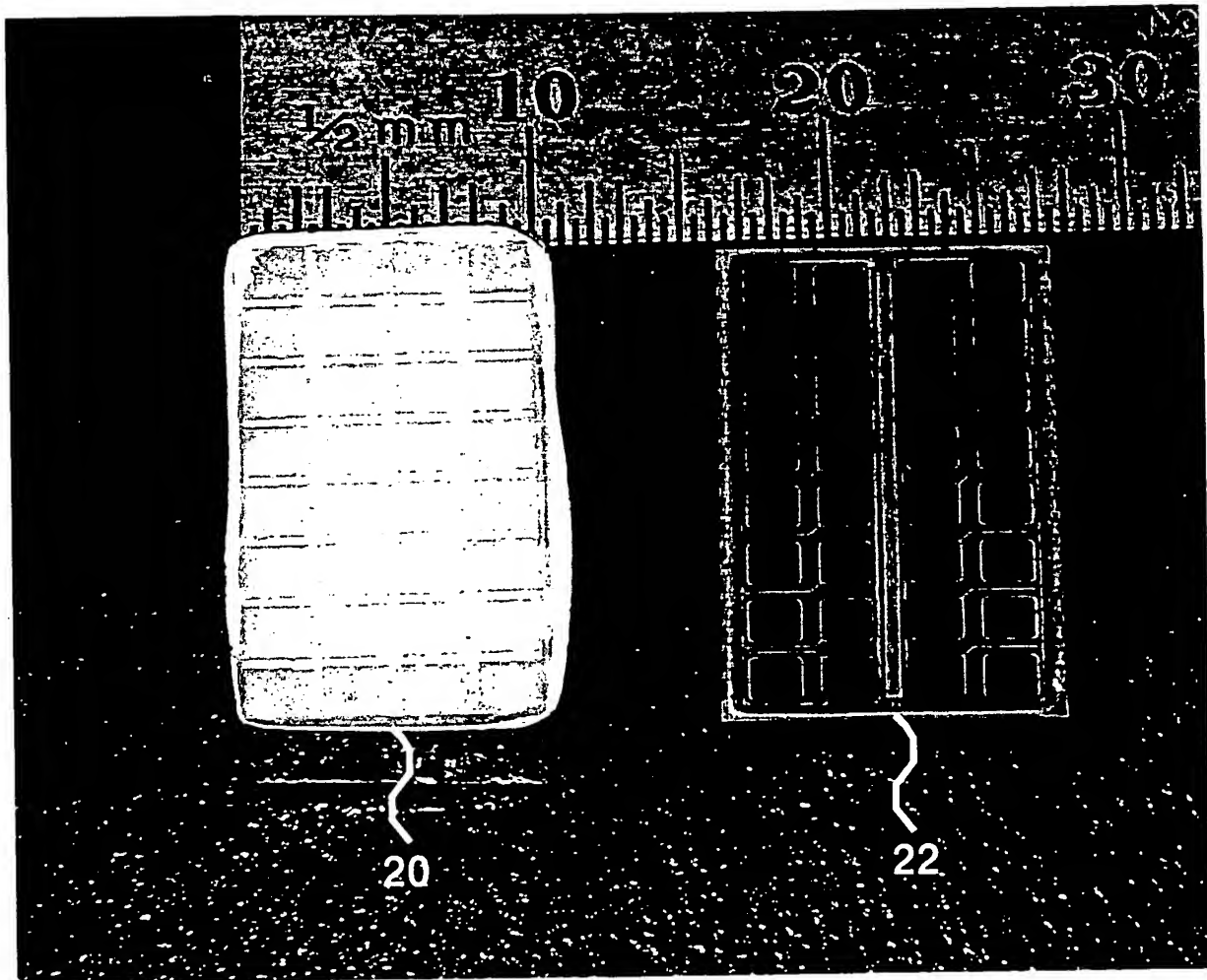
**Figure 1**



**Figure 2a**

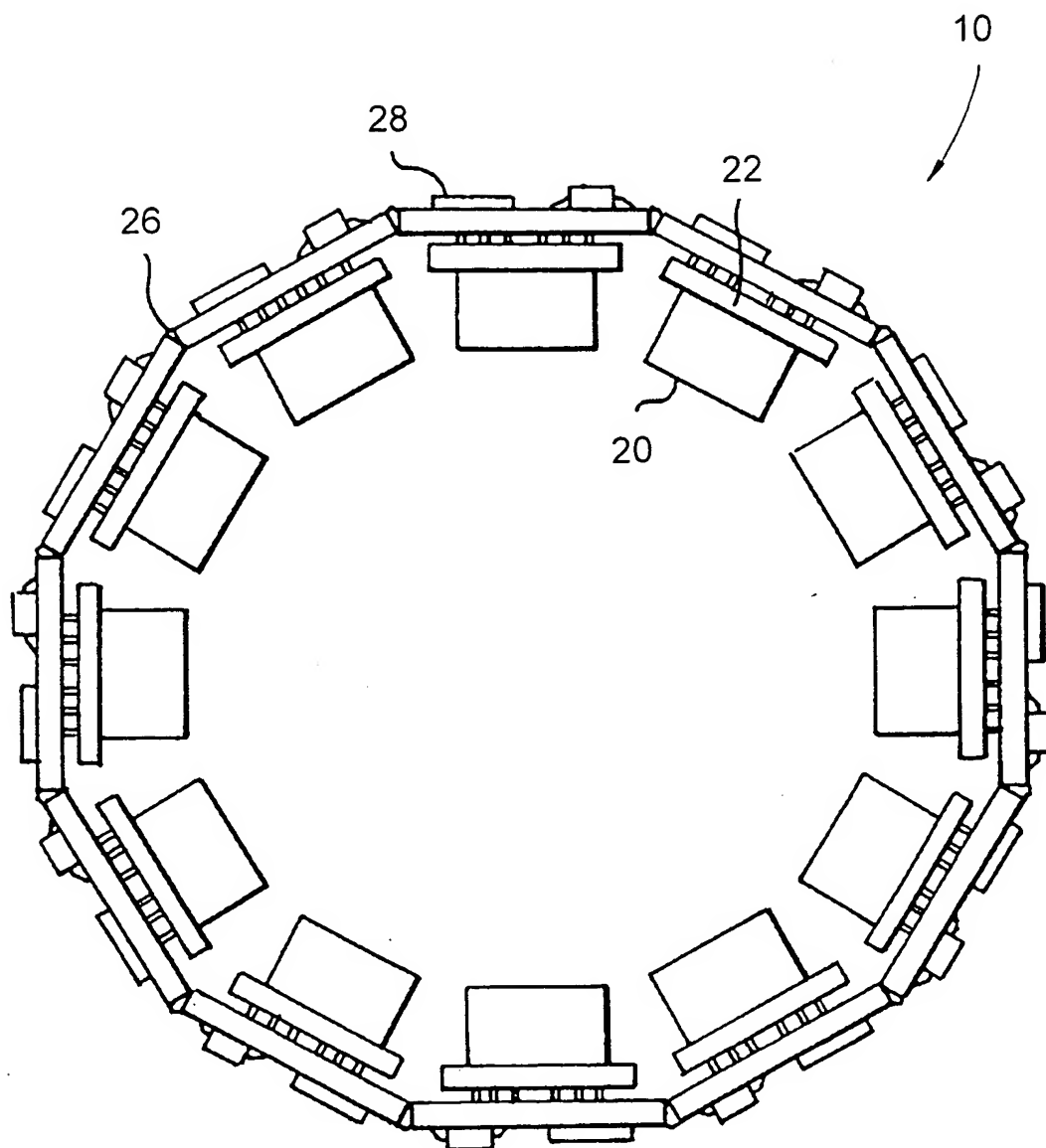


**Figure 2b**



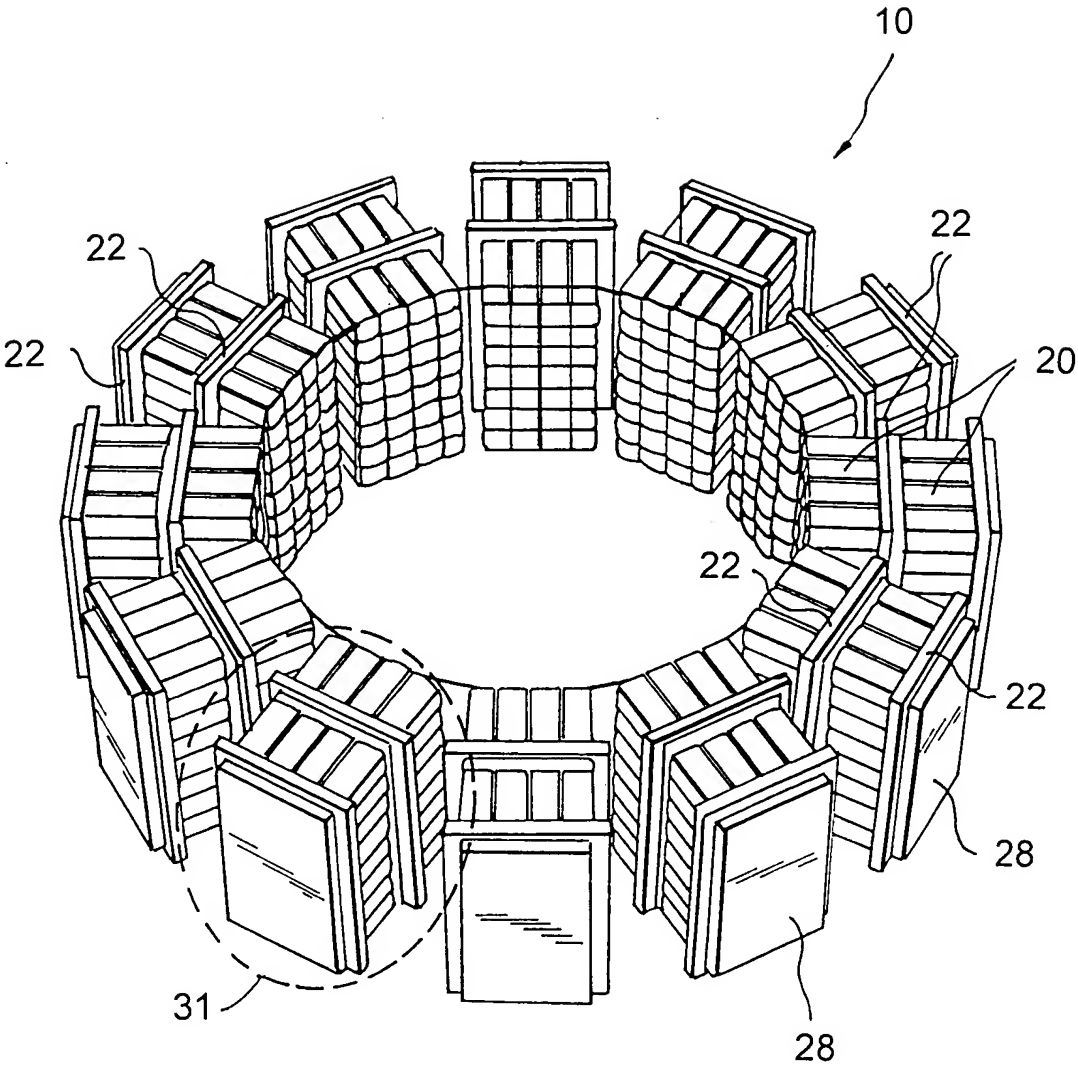
**Figure 3**

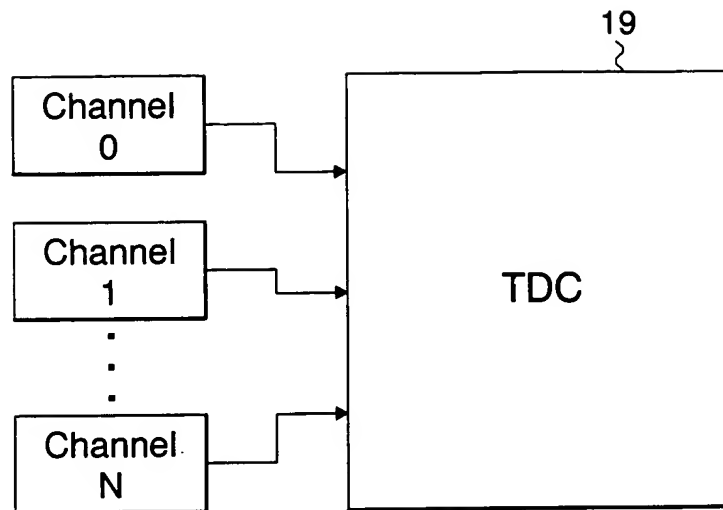
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**Figure 4**

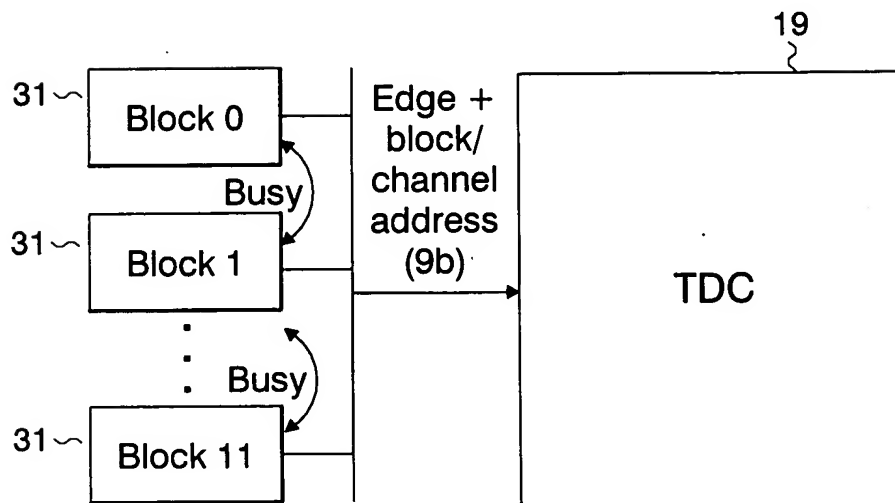
Figure 5





Individual Serial Links

**Figure 6**  
(Prior Art)



Common Serial Bus with Busy

**Figure 7**

# Serial Link Timing

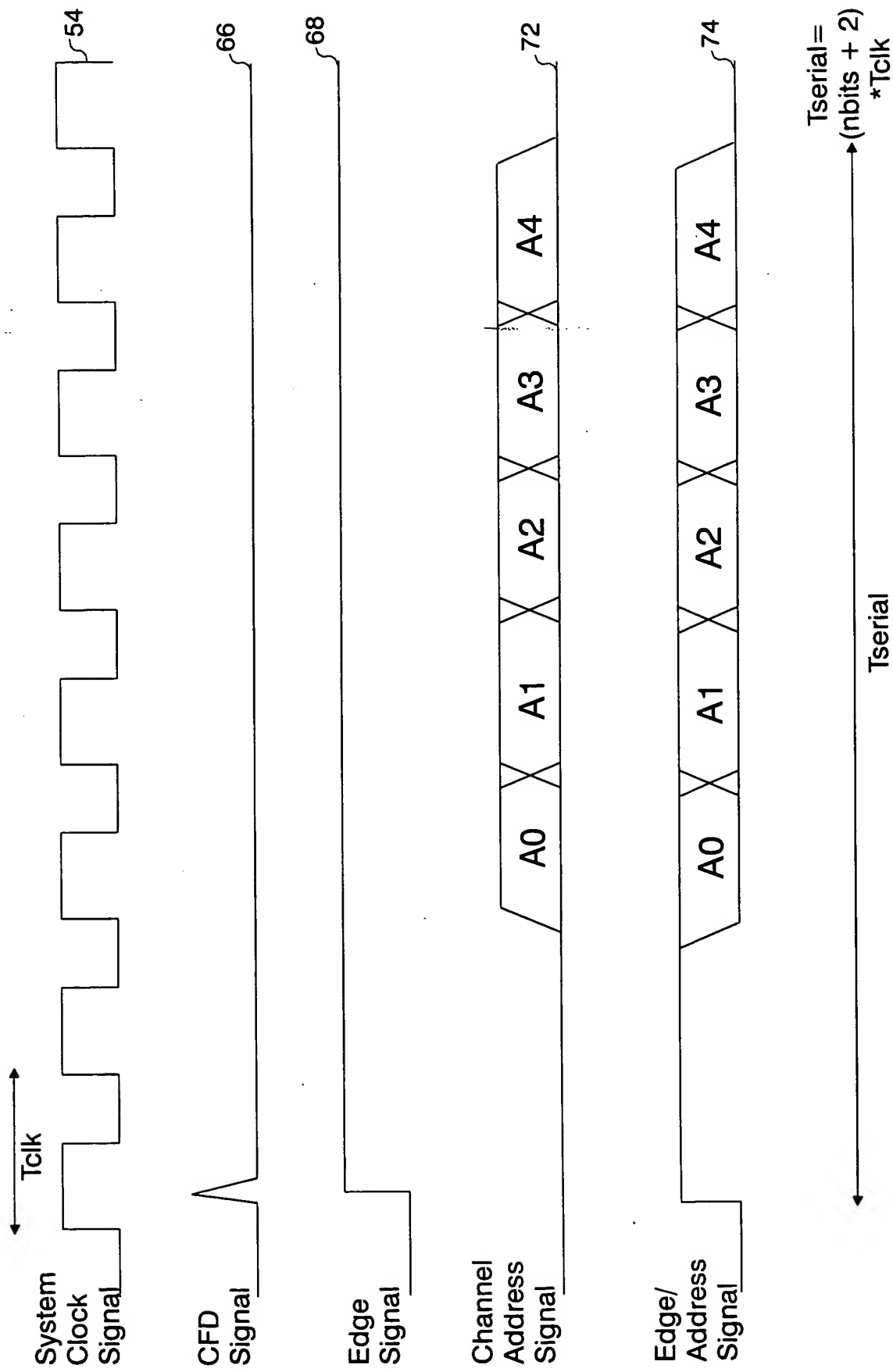
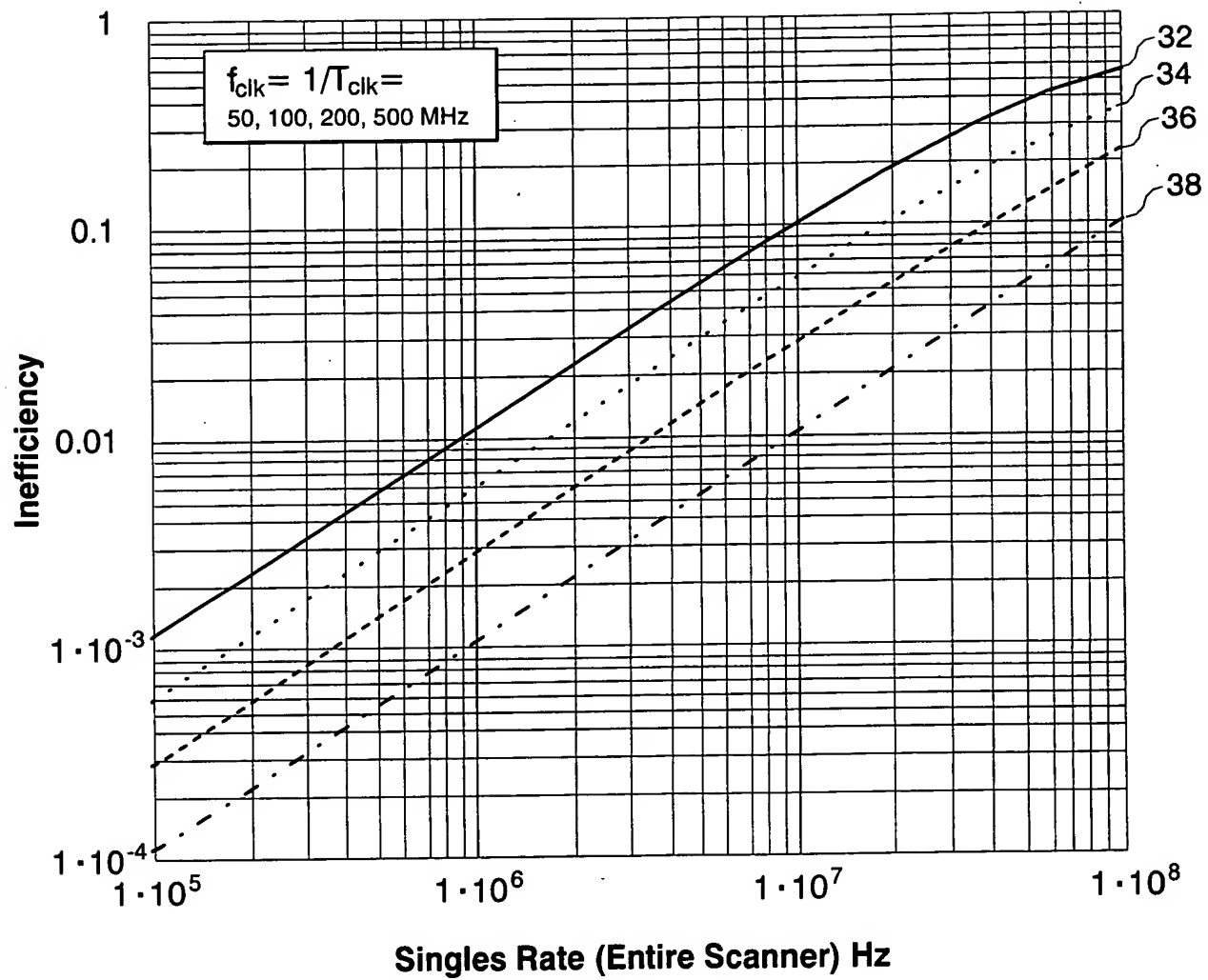


Figure 8





**Figure 9**

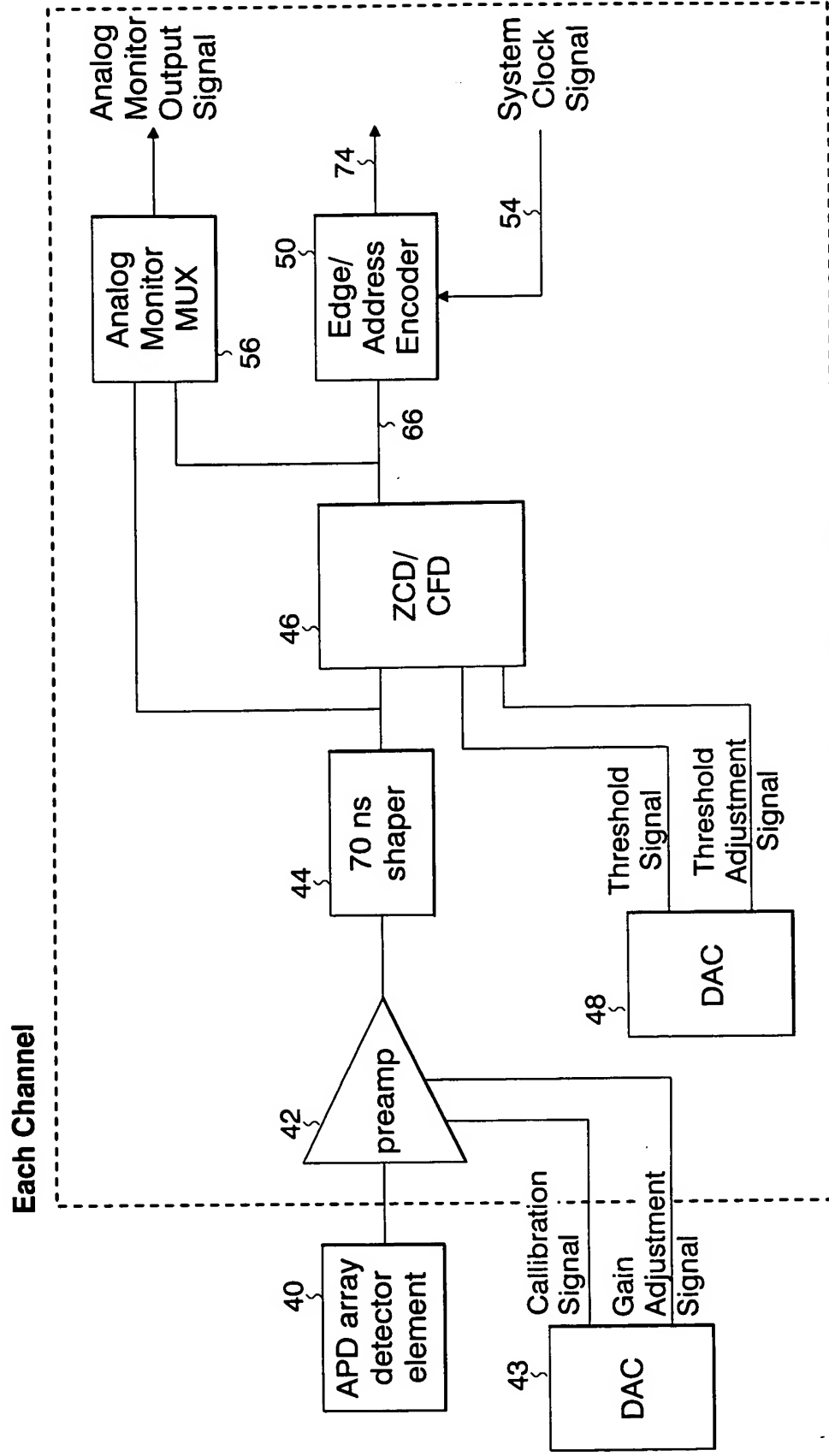
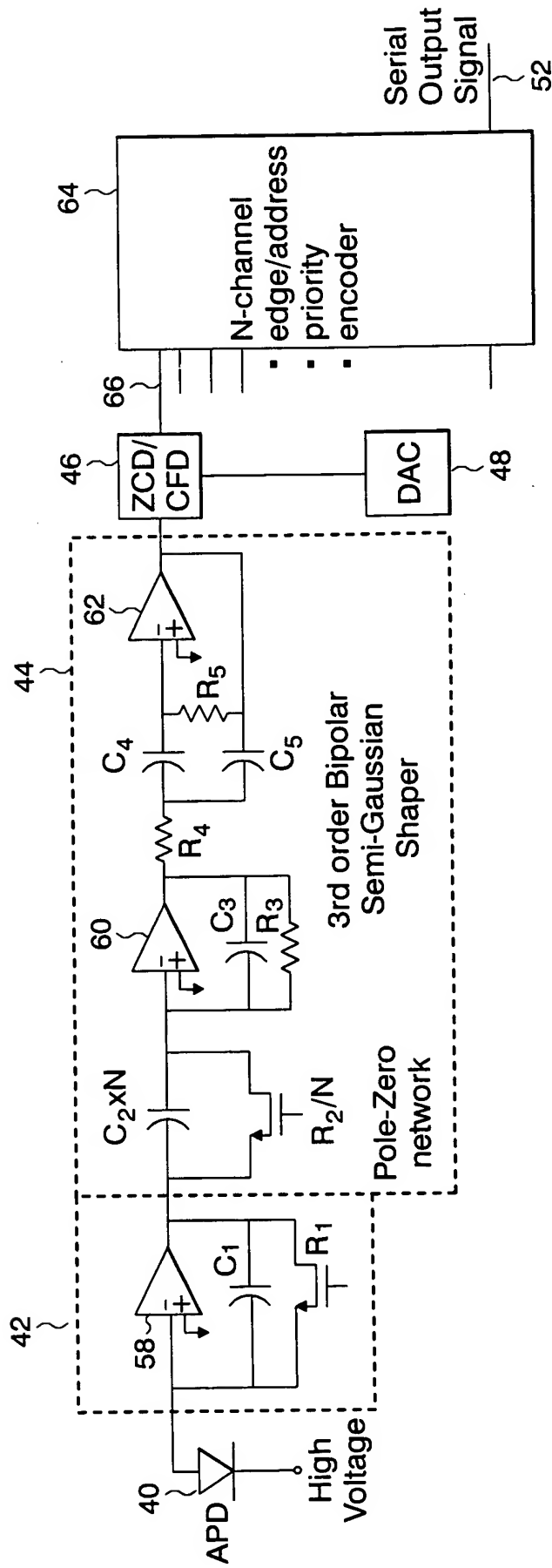


Figure 10



**Figure 11**

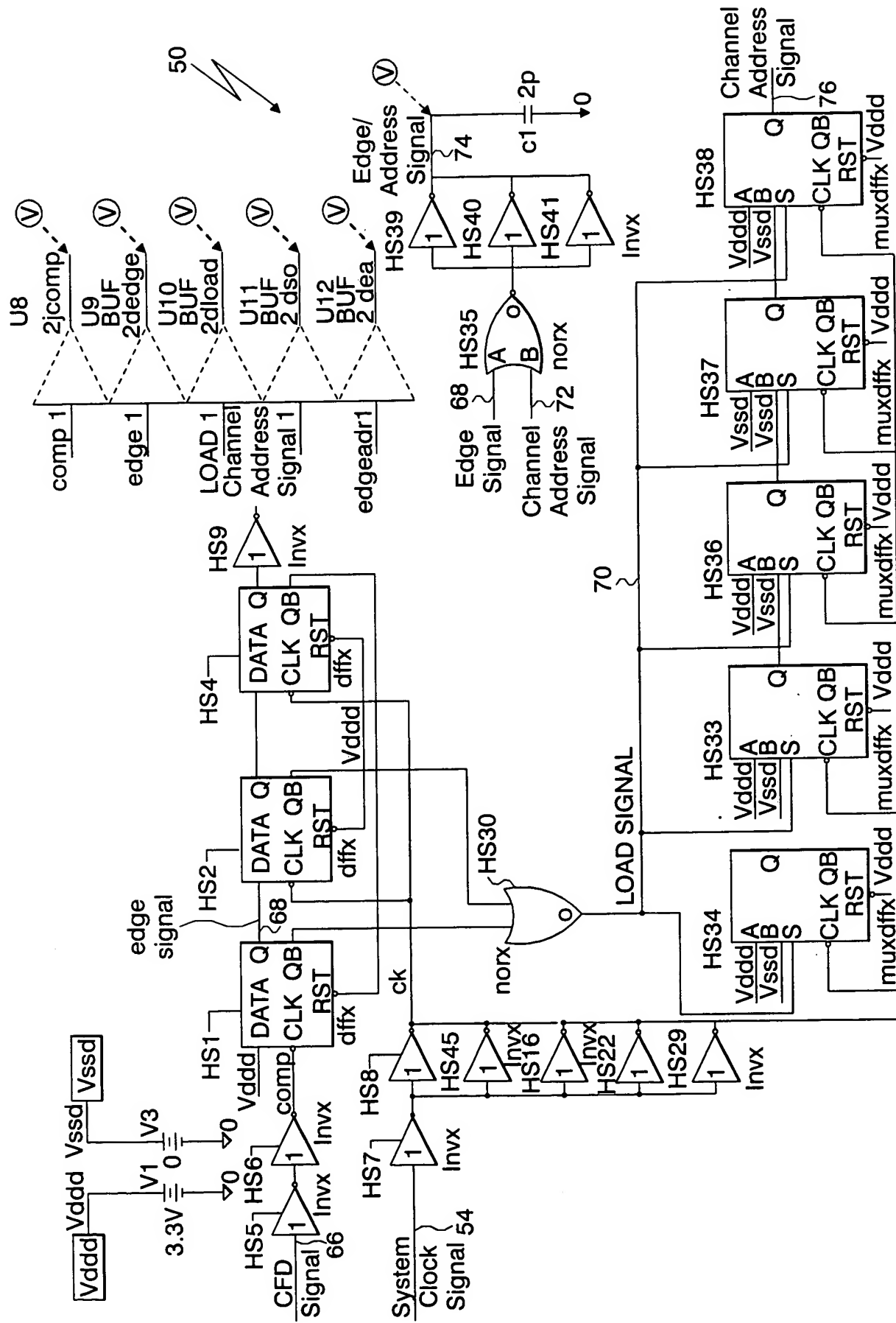


Figure 12

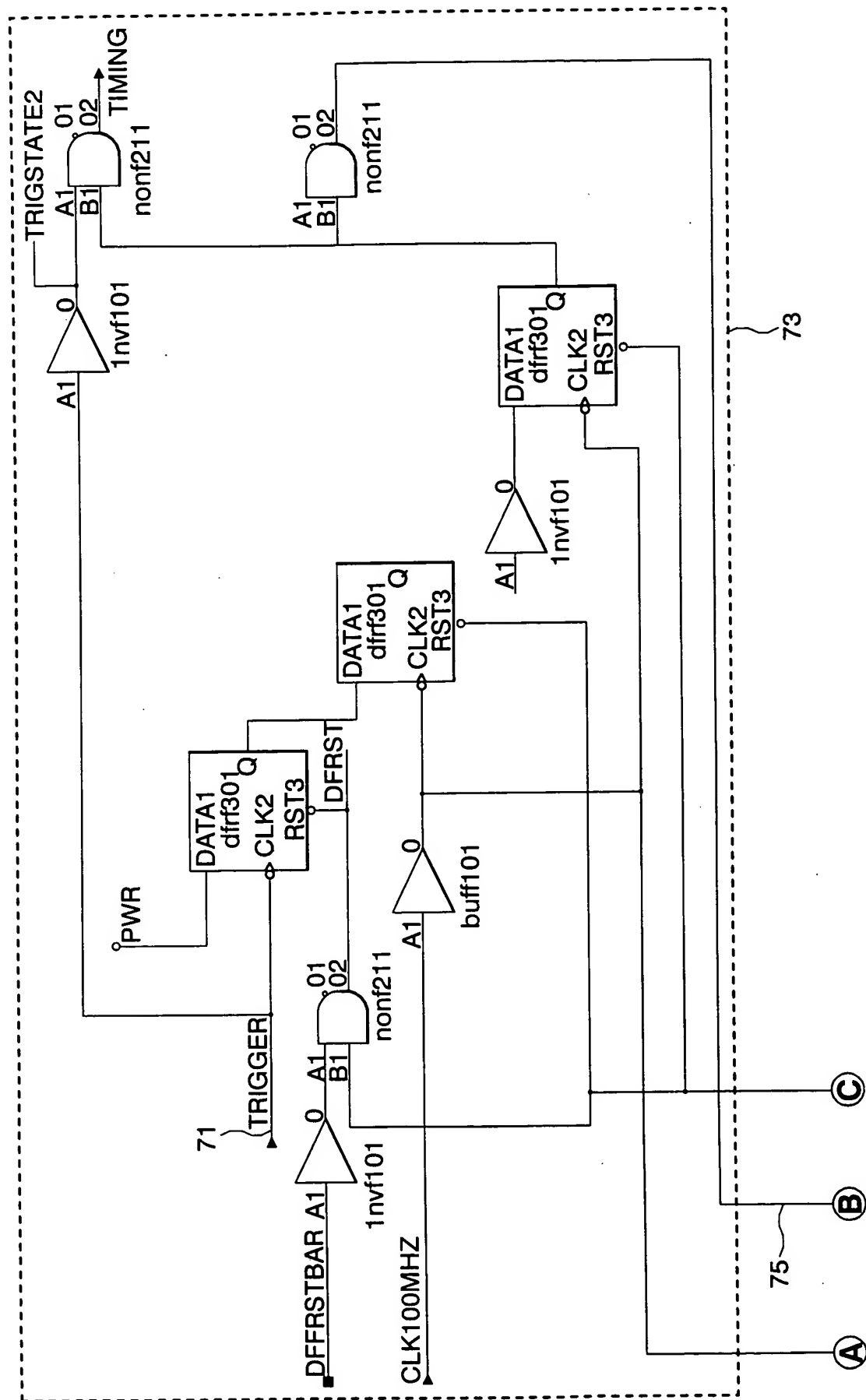
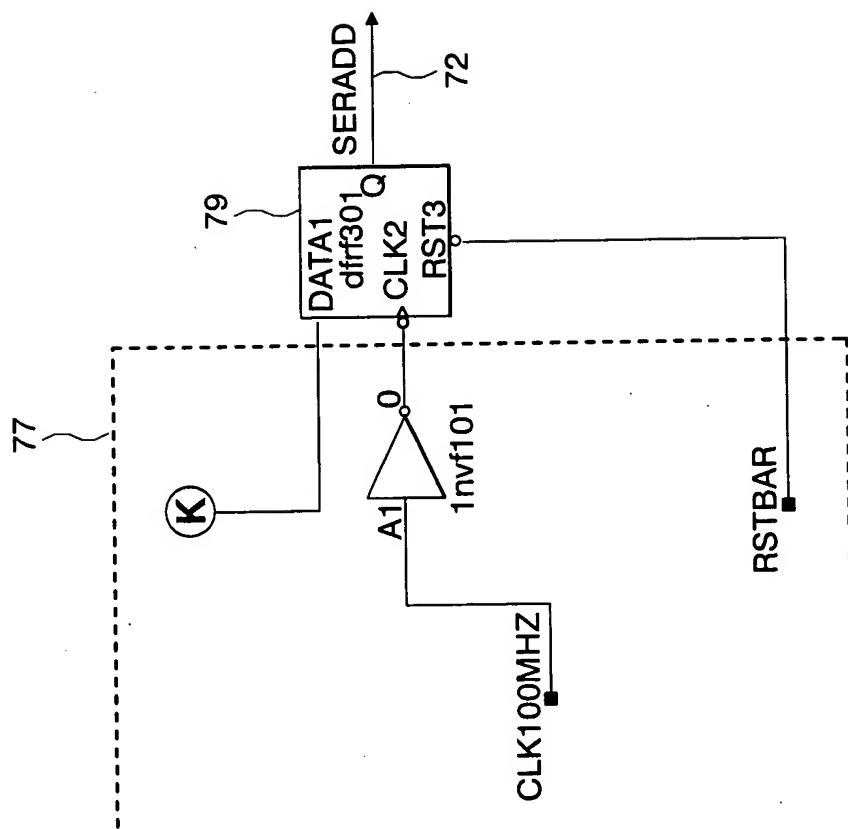


Figure 12a(1)







**Figure 12a(4)**



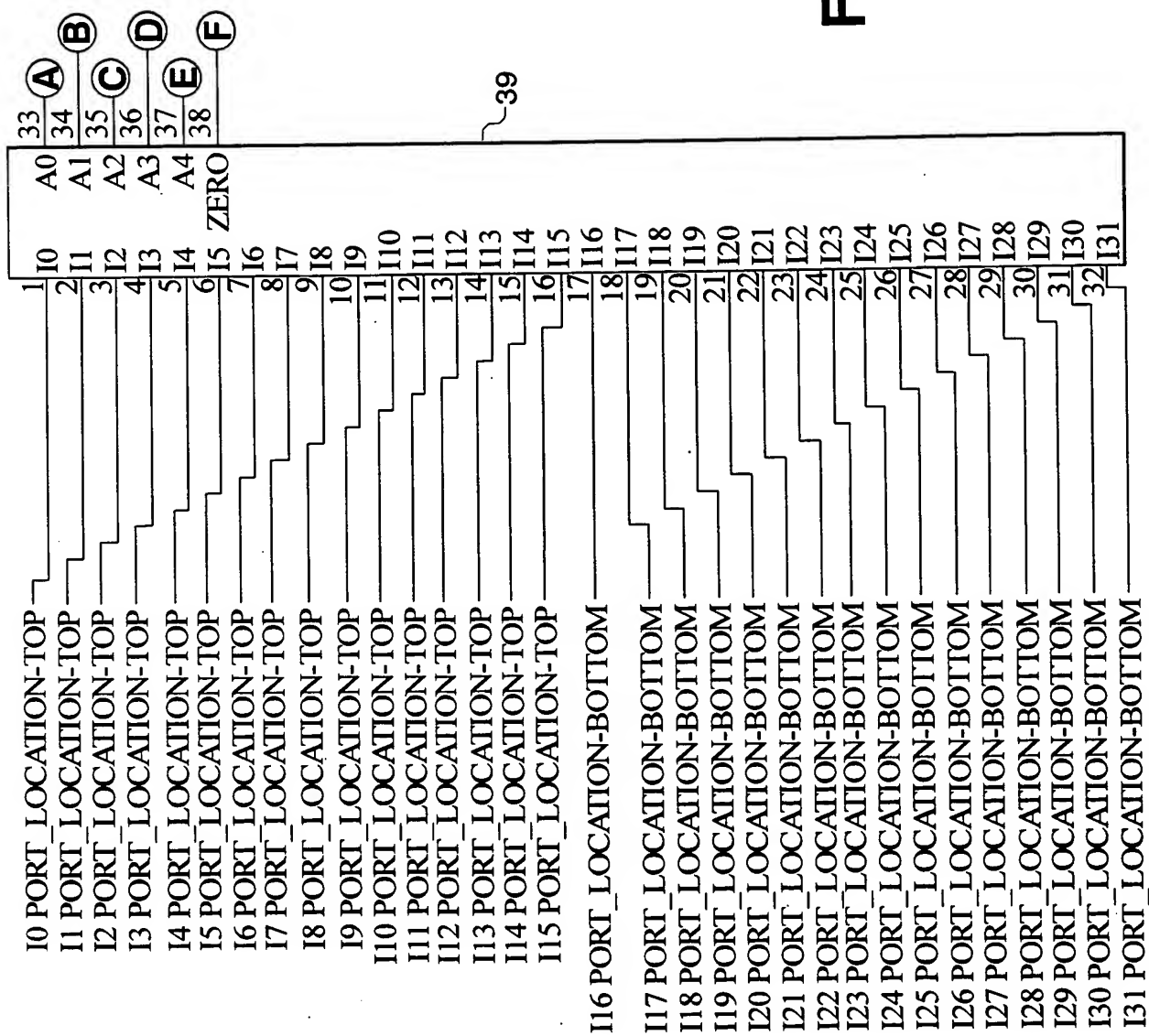


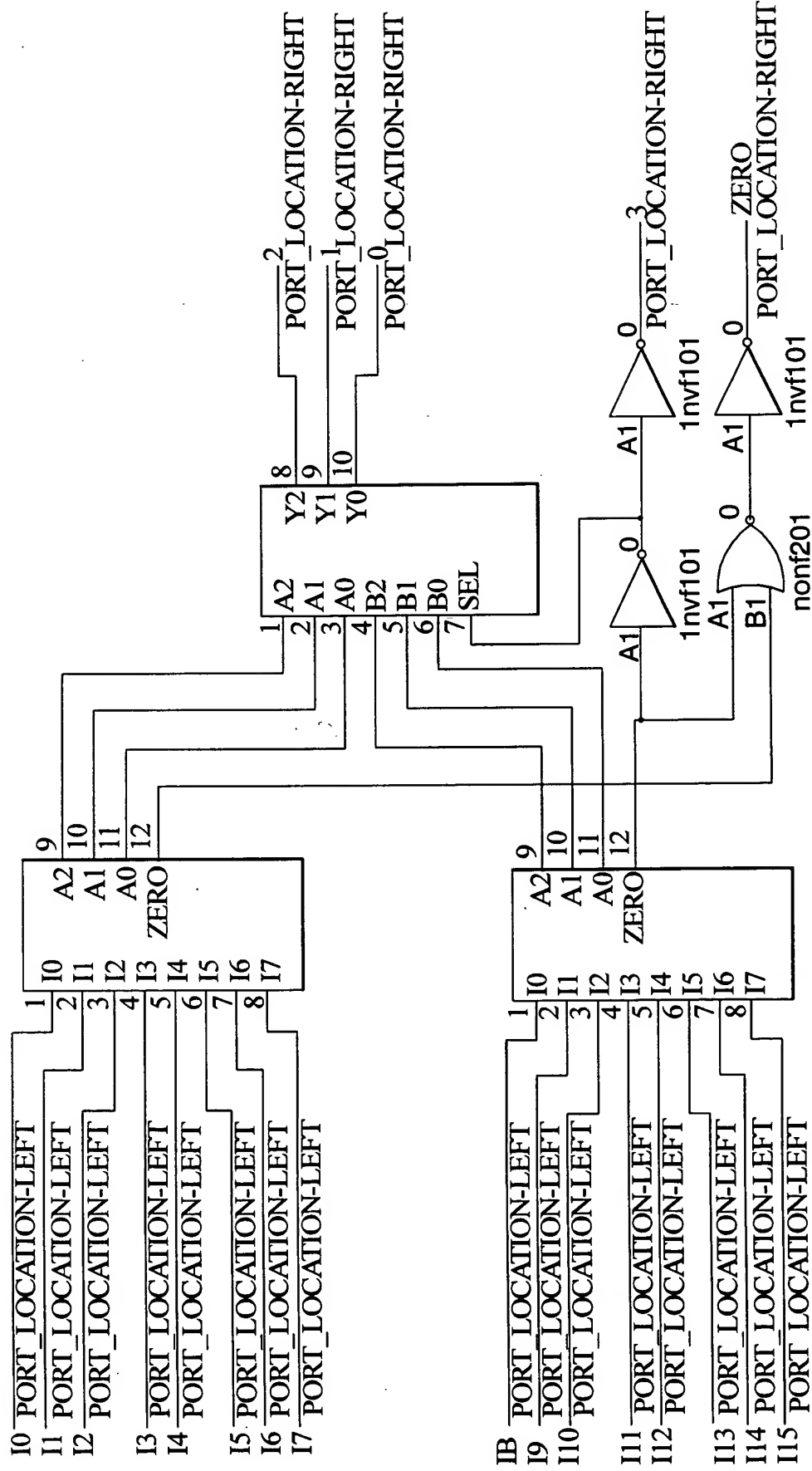
Figure 13(a)

# Figure 13(b)

Figure 13(b) is a logic diagram showing the internal structure of a 32-bit register. The diagram includes the following components and connections:

- Register Block (Top):**
  - Inputs:** SELECT (A0, A1, A2, A3, A4), CHAND, and RSTBAR.
  - Outputs:** PORT\_LOCATION-80, PORT\_LOCATION-40, and PORT\_LOCATION-0.
- Multiplexer Block (Bottom):**
  - Inputs:** SELECT (SEL0, SEL1, SEL2, SEL3, SEL4), TRIGGER, RSTBAR, and CLK.
  - Outputs:** PORT\_LOCATION-80, PORT\_LOCATION-40, and PORT\_LOCATION-0.
- Connections:**
  - The **SELECT** inputs of the register are connected to the **SELECT** inputs of the multiplexer.
  - The **CHAND** input of the register is connected to the **TRIGGER** input of the multiplexer.
  - The **RSTBAR** input of the register is connected to the **RSTBAR** input of the multiplexer.
  - The **CLK** input of the register is connected to the **CLK** input of the multiplexer.
  - The **PORT\_LOCATION-80** output of the register is connected to the **PORT\_LOCATION-80** output of the multiplexer.
  - The **PORT\_LOCATION-40** output of the register is connected to the **PORT\_LOCATION-40** output of the multiplexer.
  - The **PORT\_LOCATION-0** output of the register is connected to the **PORT\_LOCATION-0** output of the multiplexer.

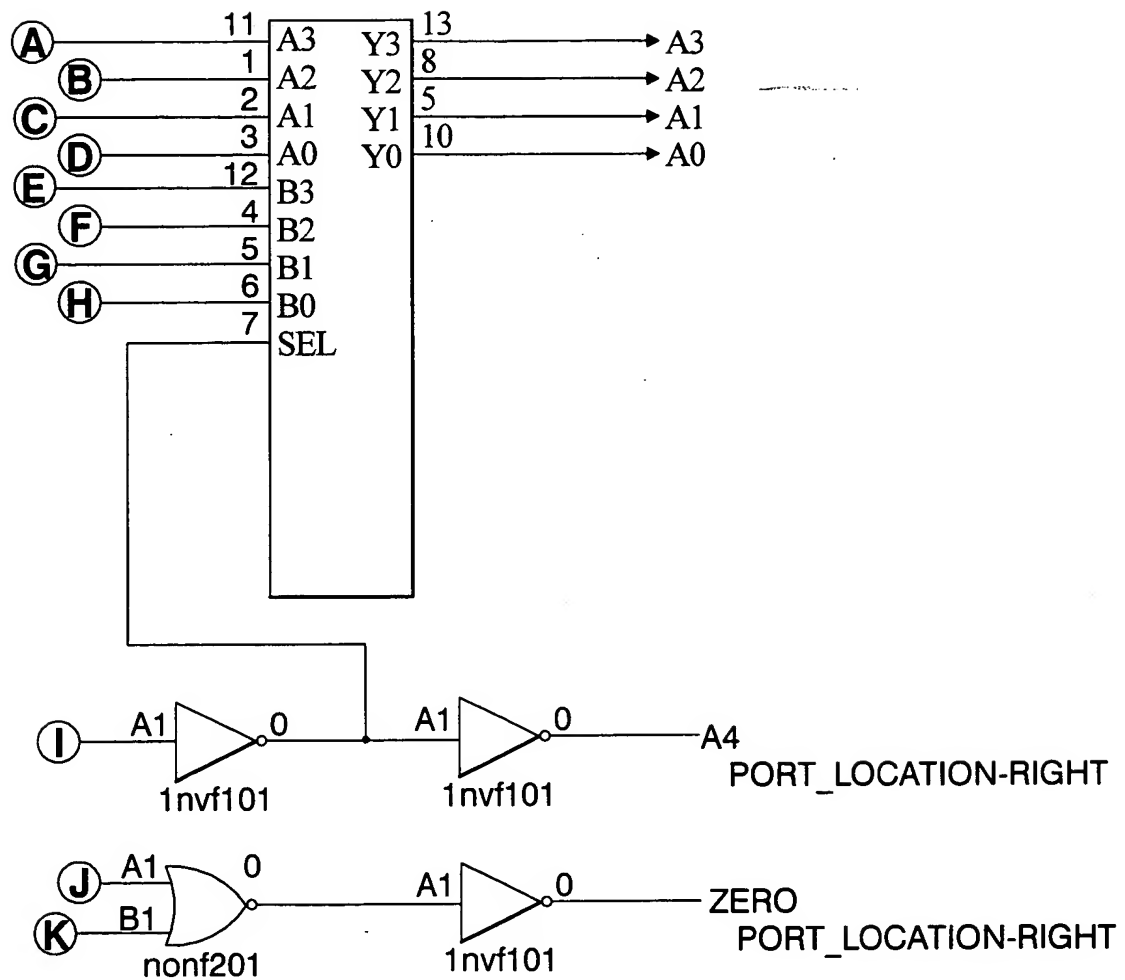
buff101 on this level to be replaced by a cascaded inverter buffer



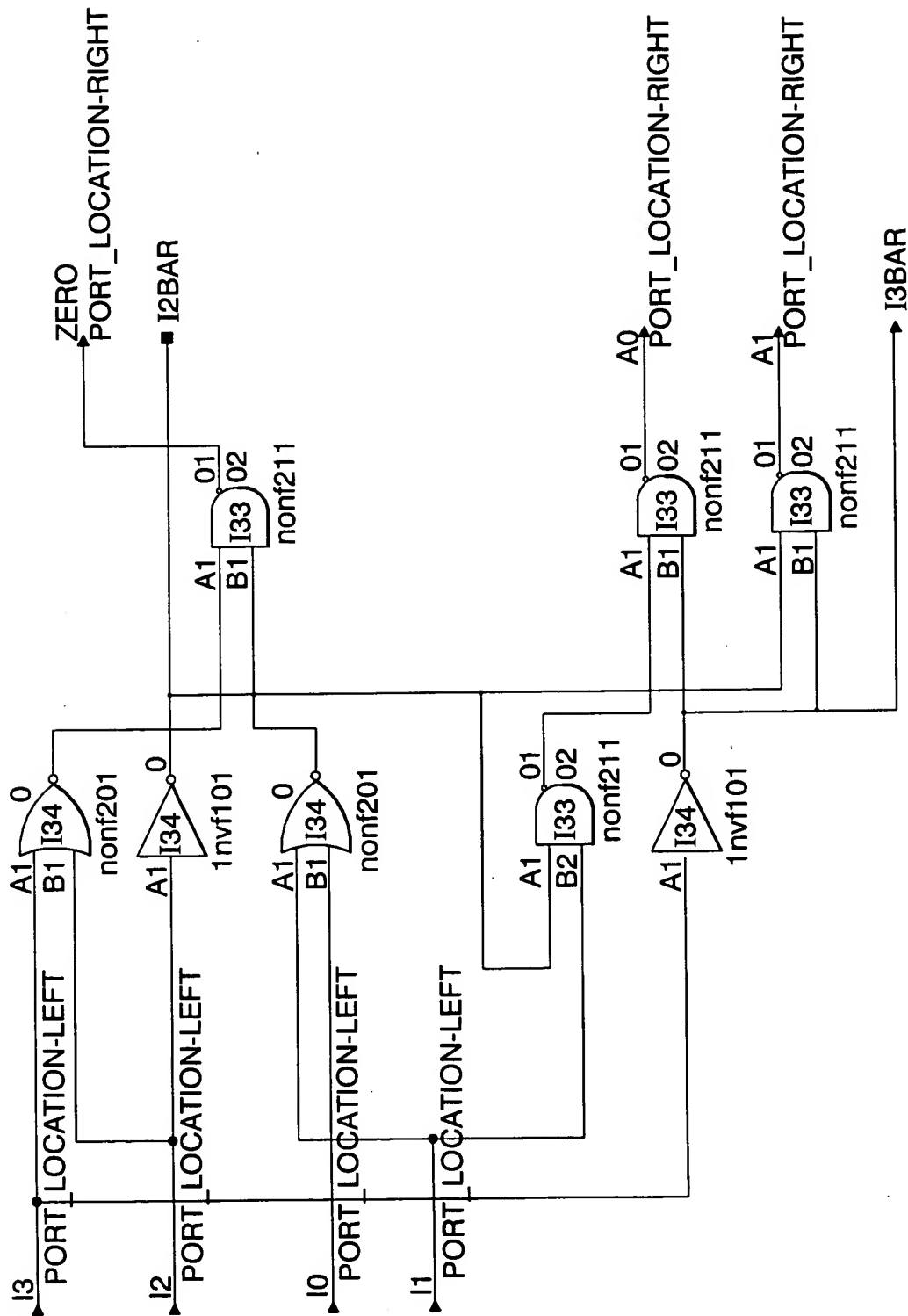
**Figure 14**



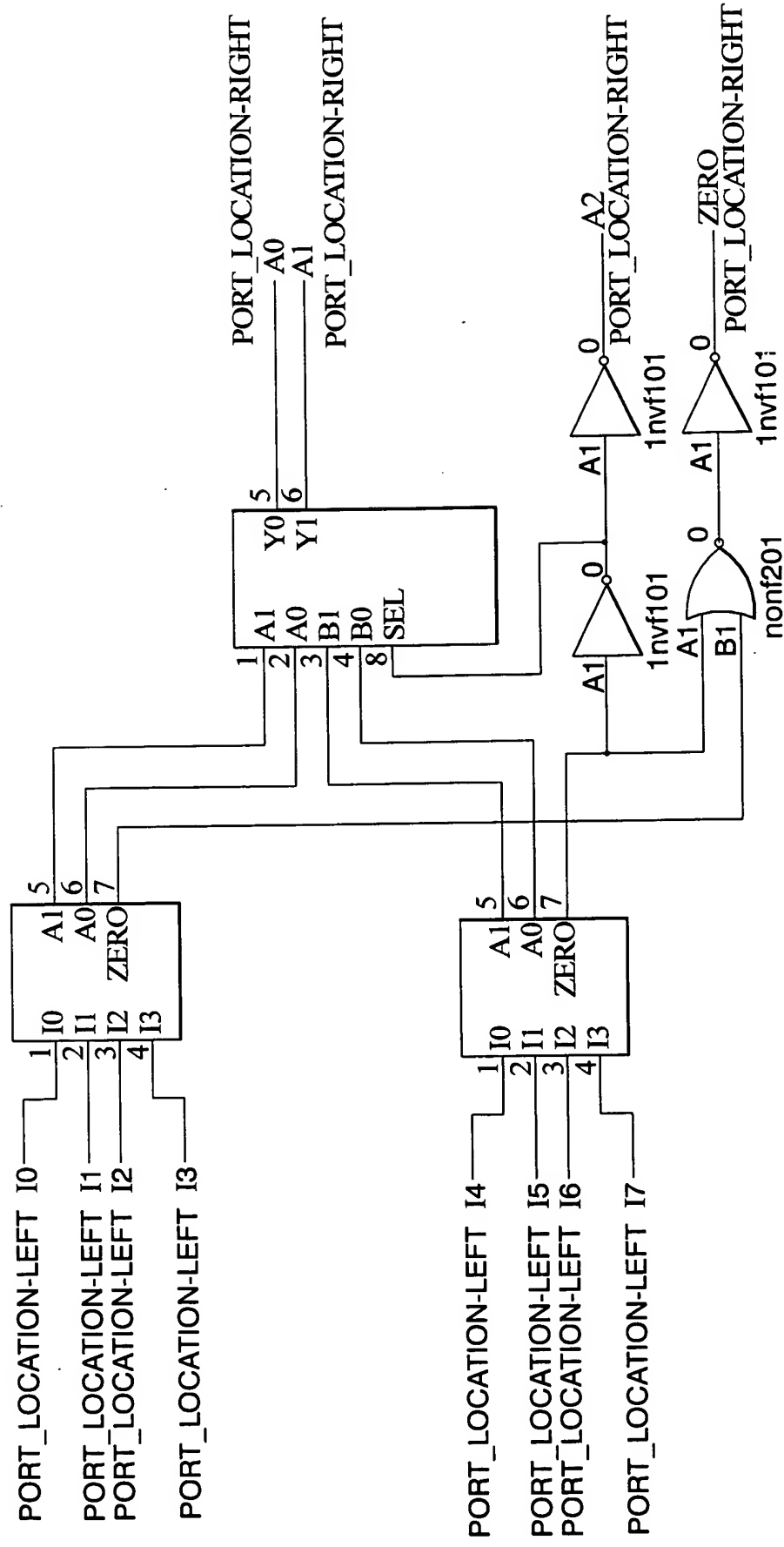
### Figure 15(a)



**Figure 15(b)**



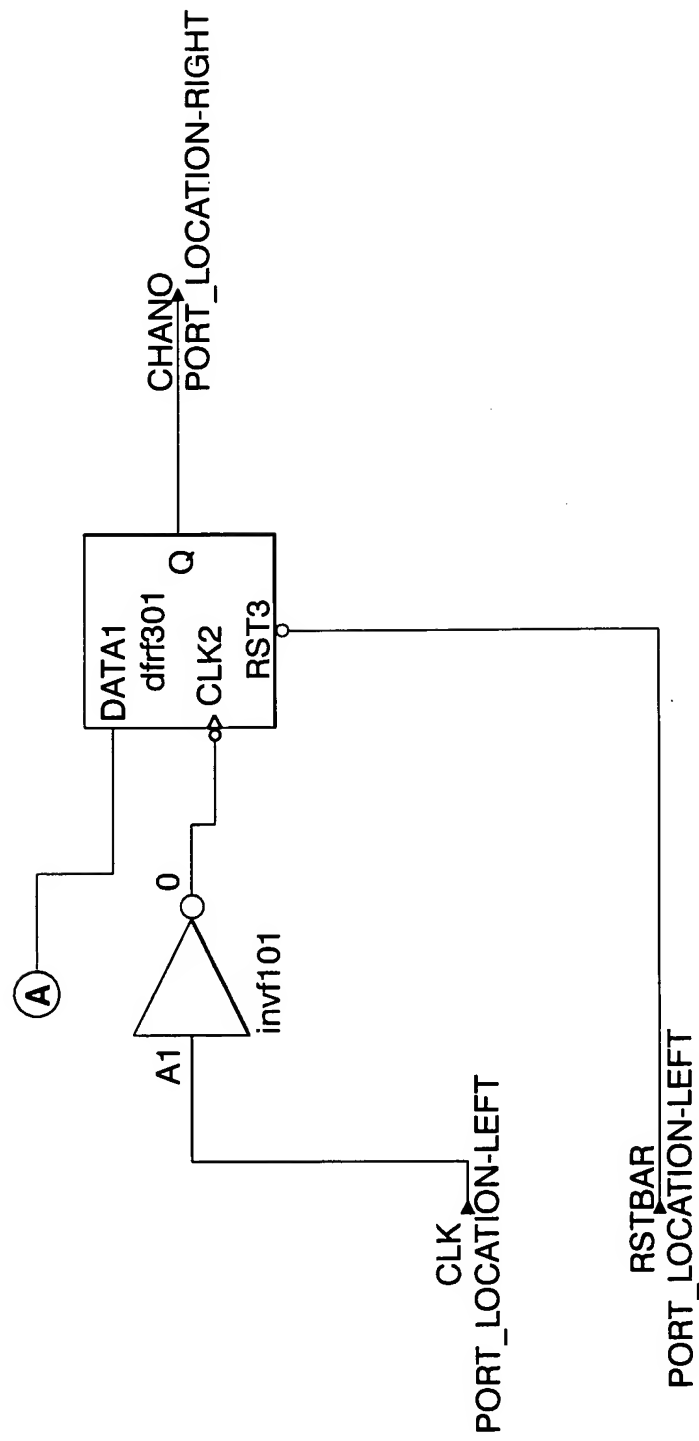
## Figure 16



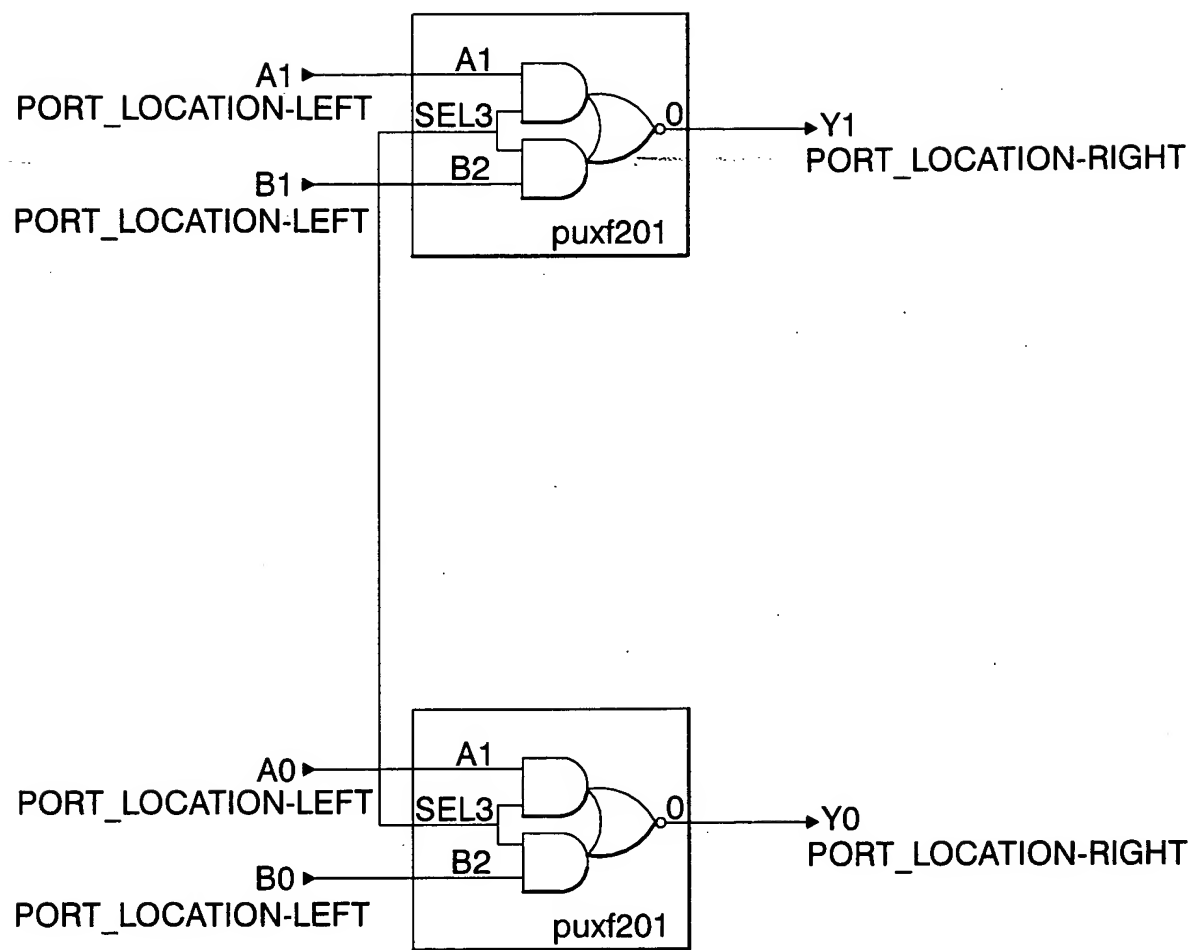
**Figure 17**



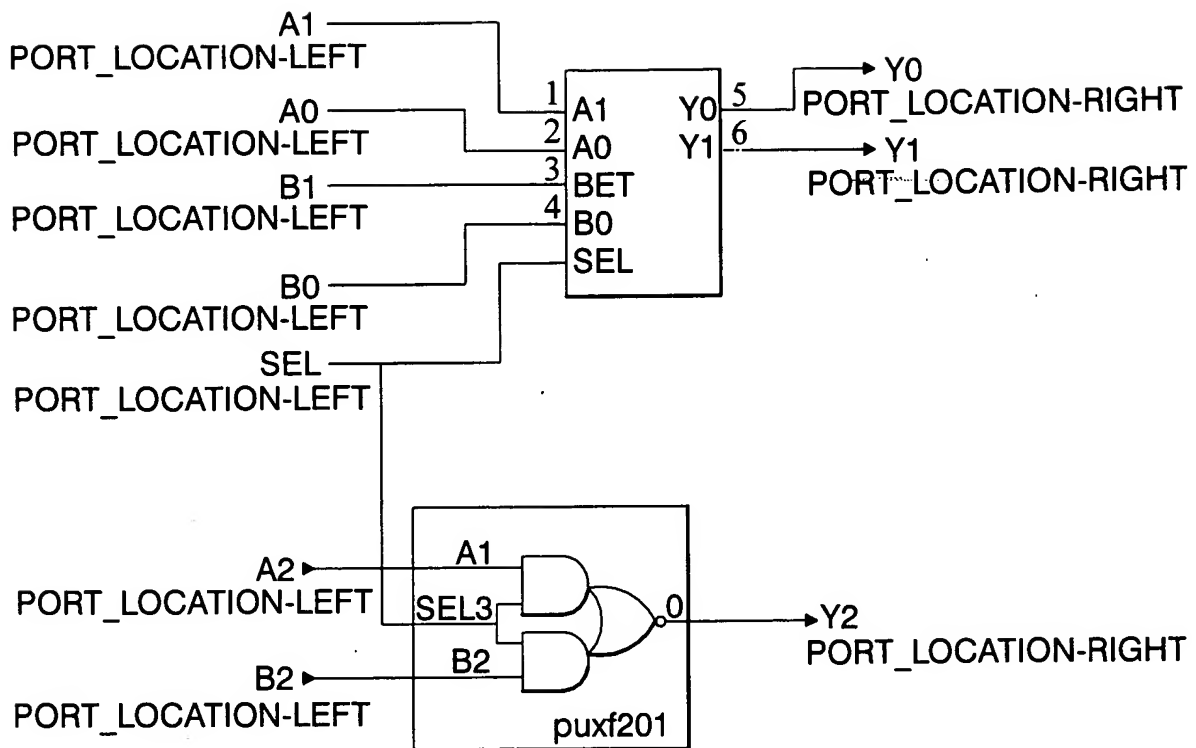




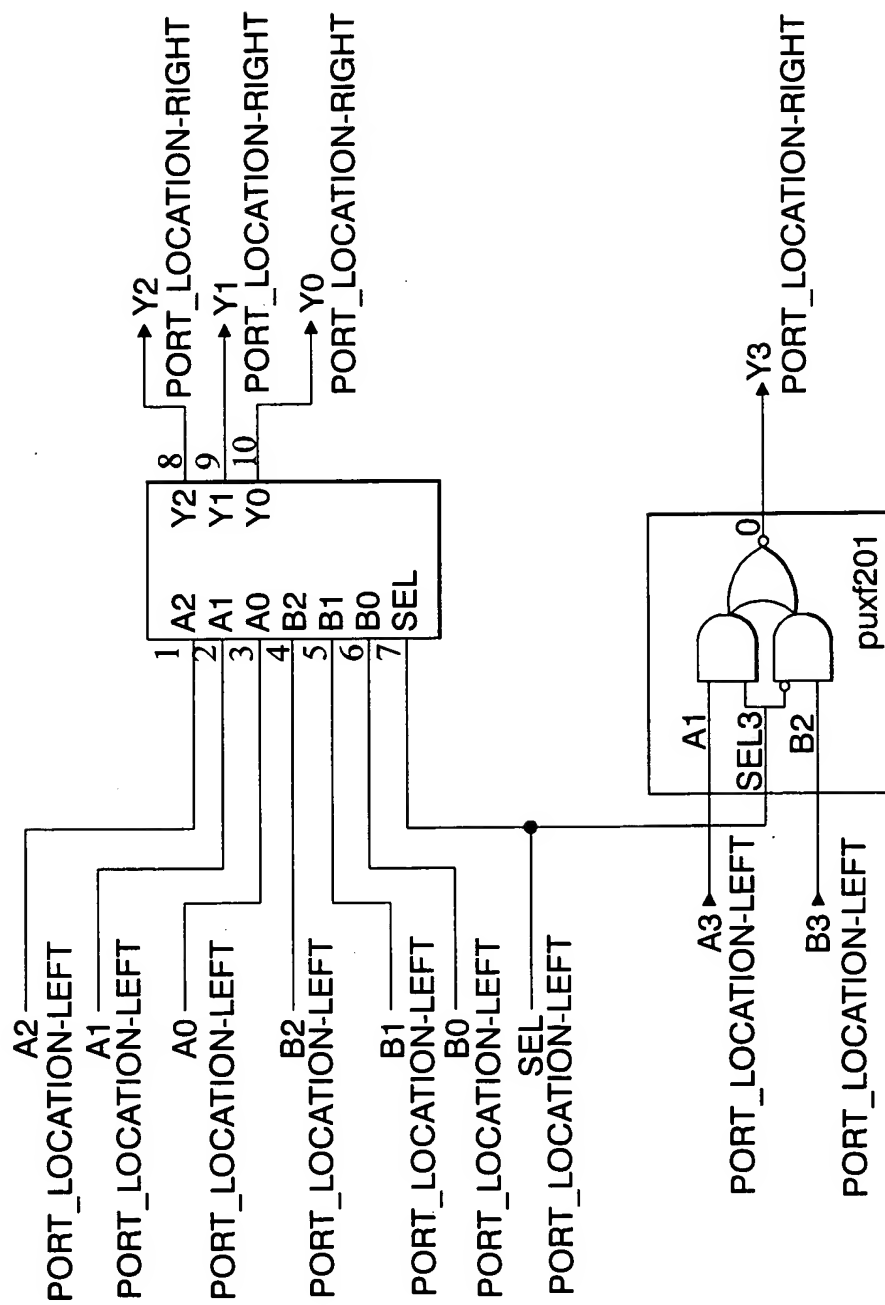
**Figure 18(b)**



**Figure 19**



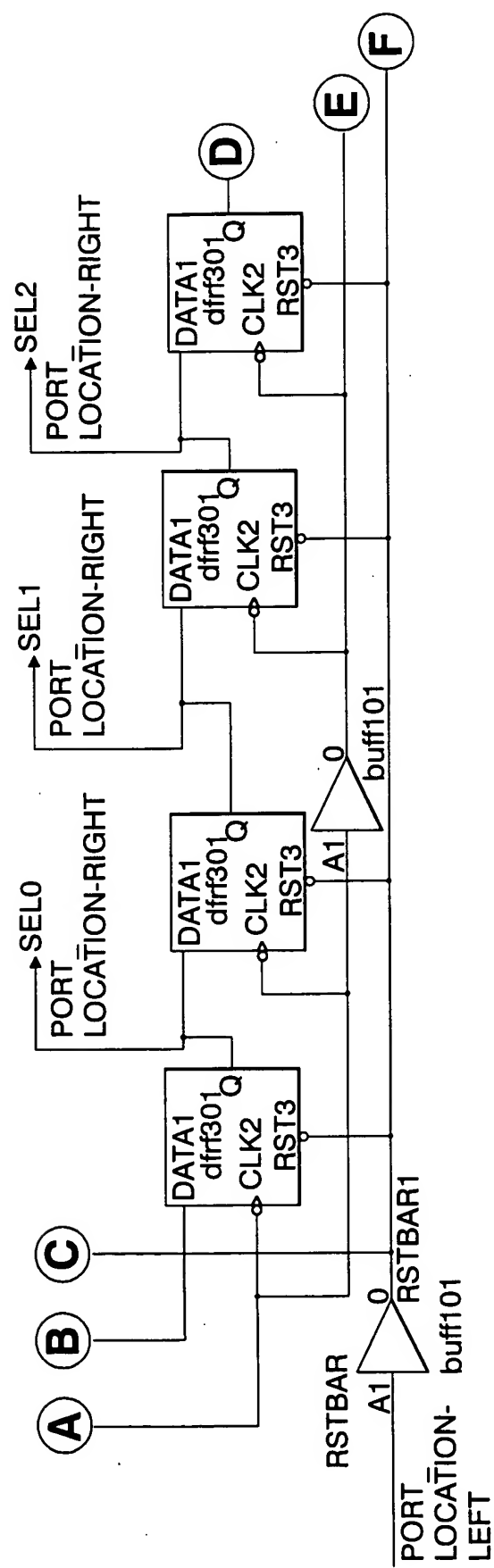
**Figure 20**

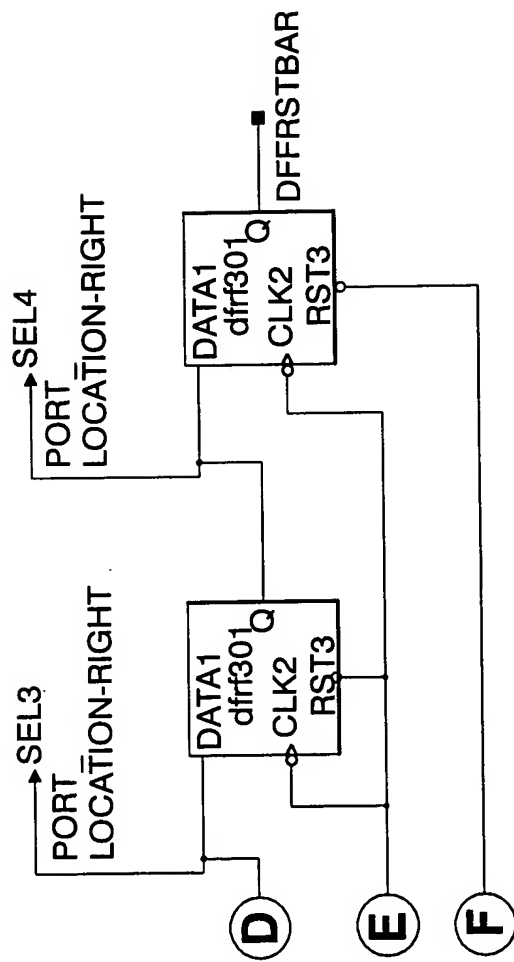


**Figure 21**

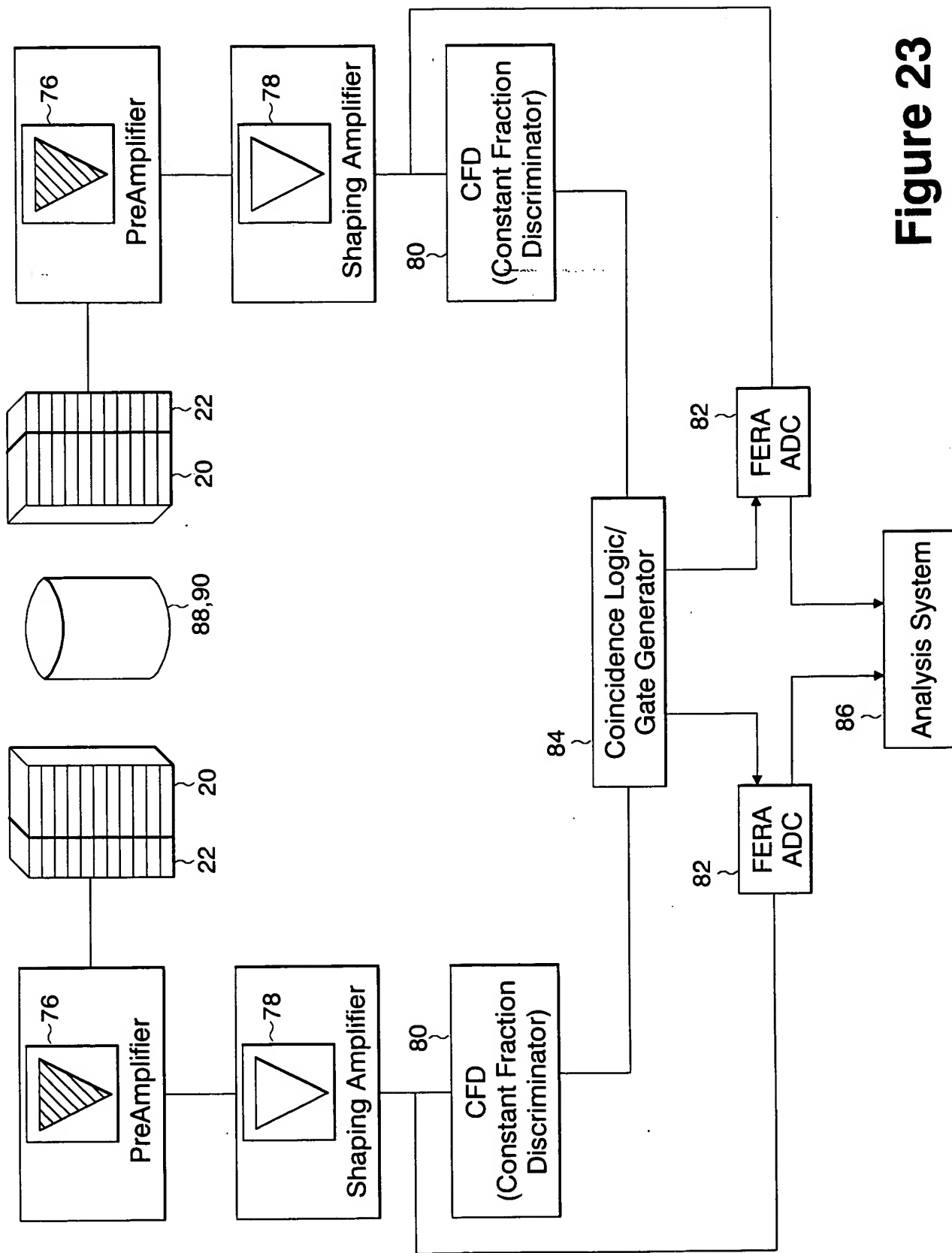


## Figure 22(a)



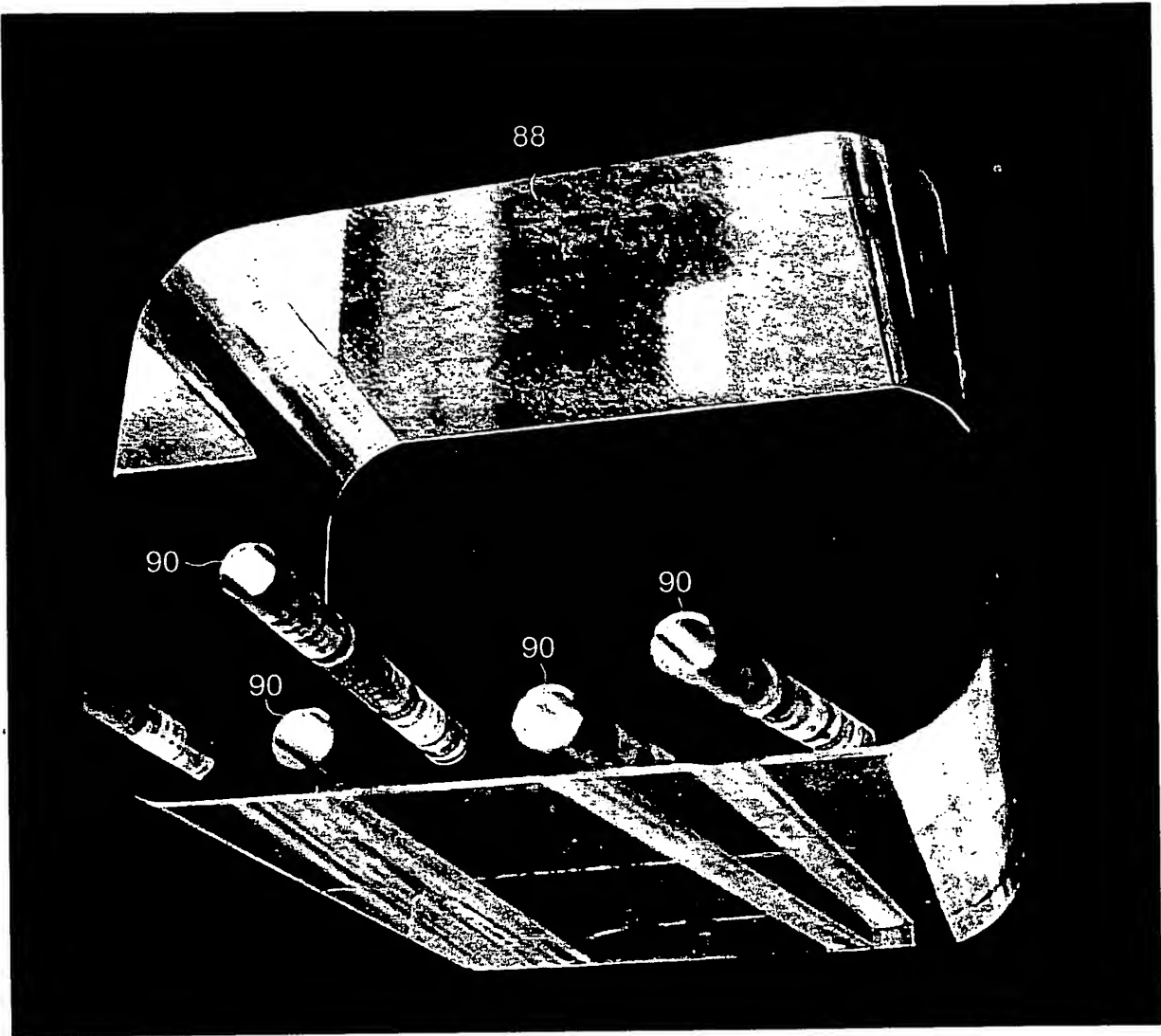


**Figure 22(c)**



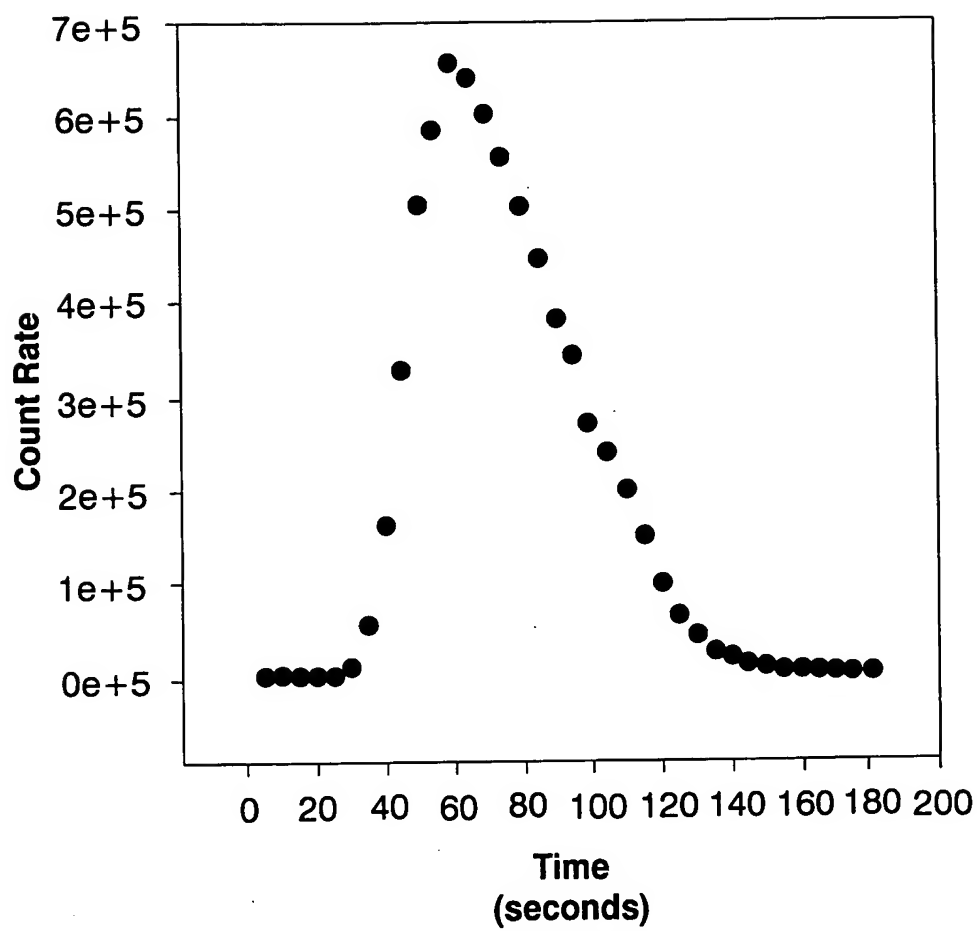
**Figure 23**





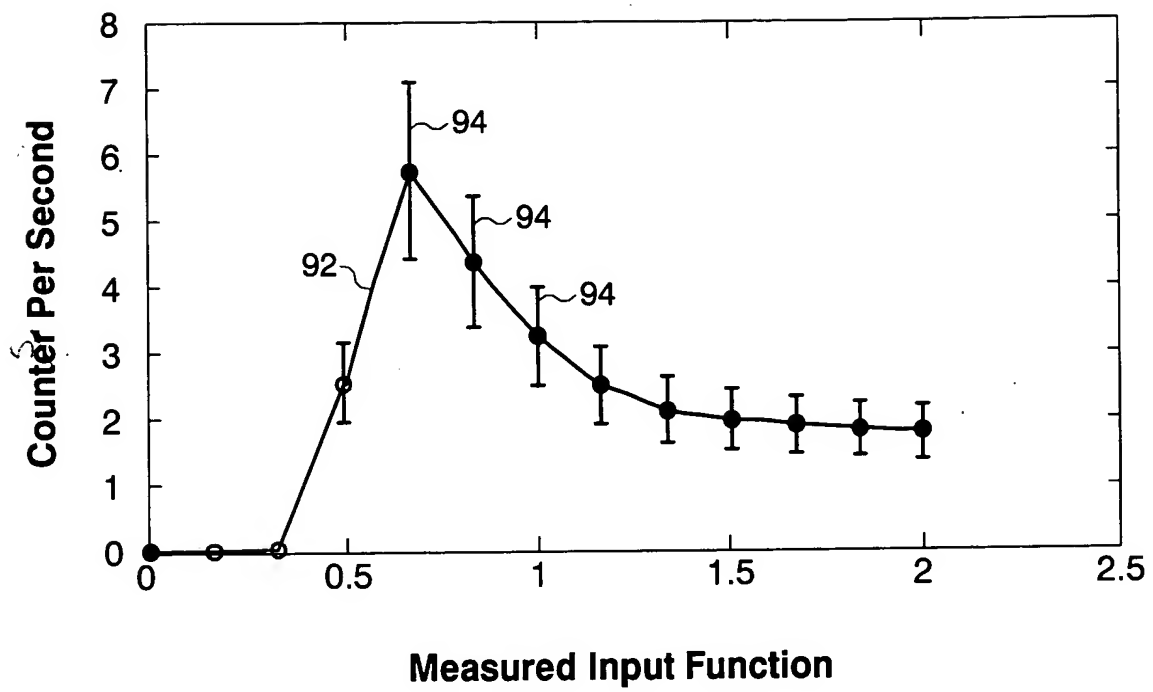
**Figure 24**

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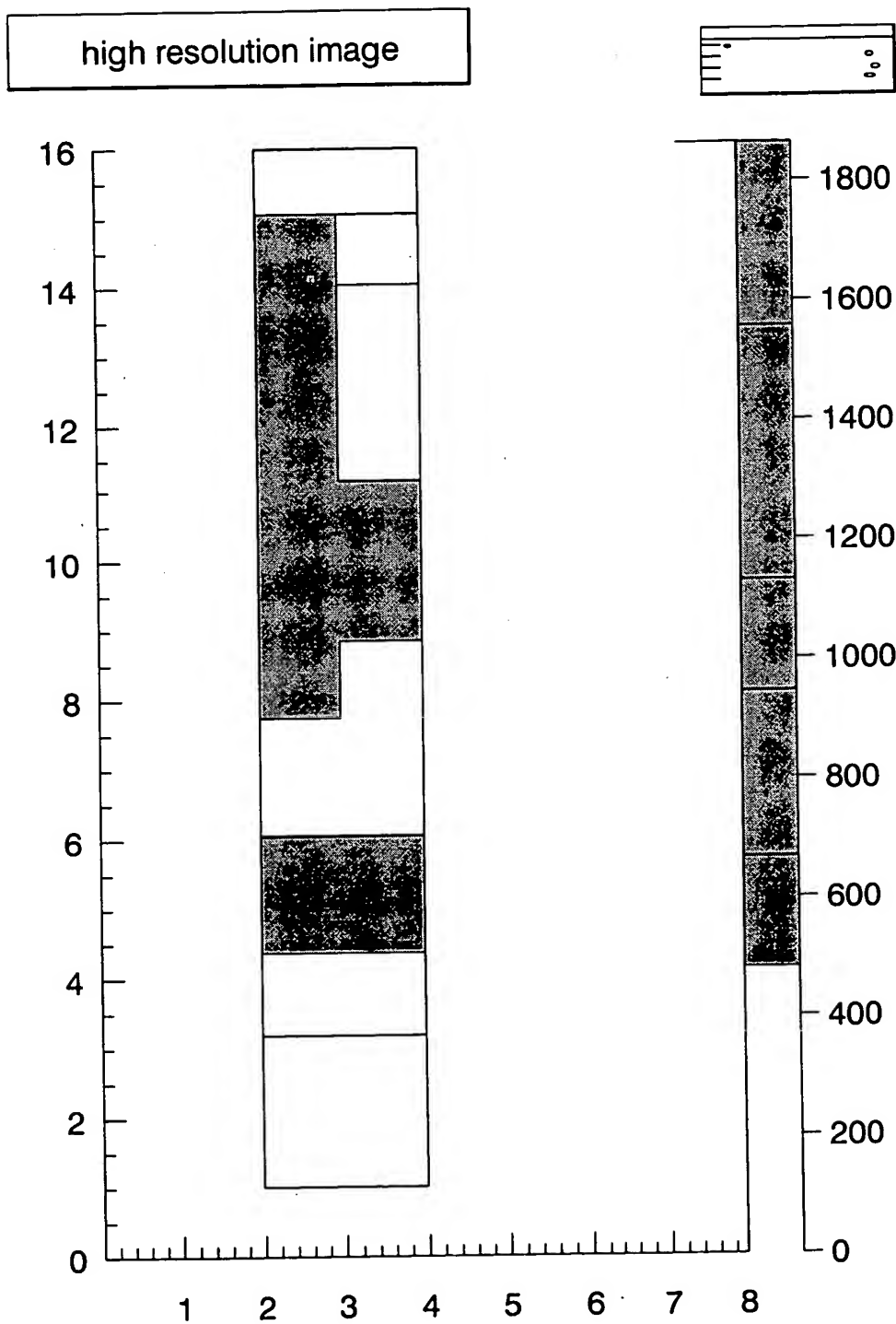


Input Function

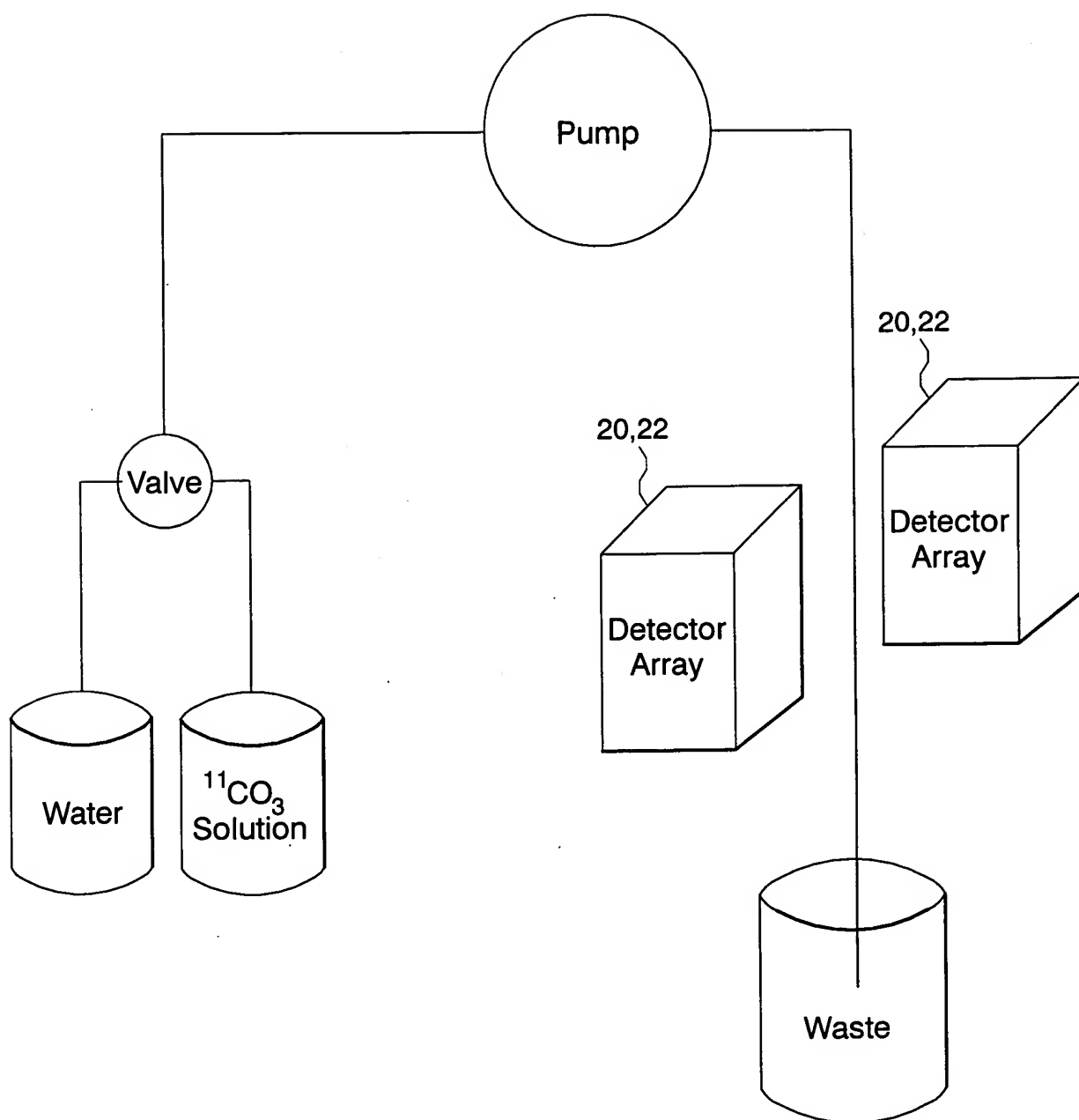
**Figure 24a**



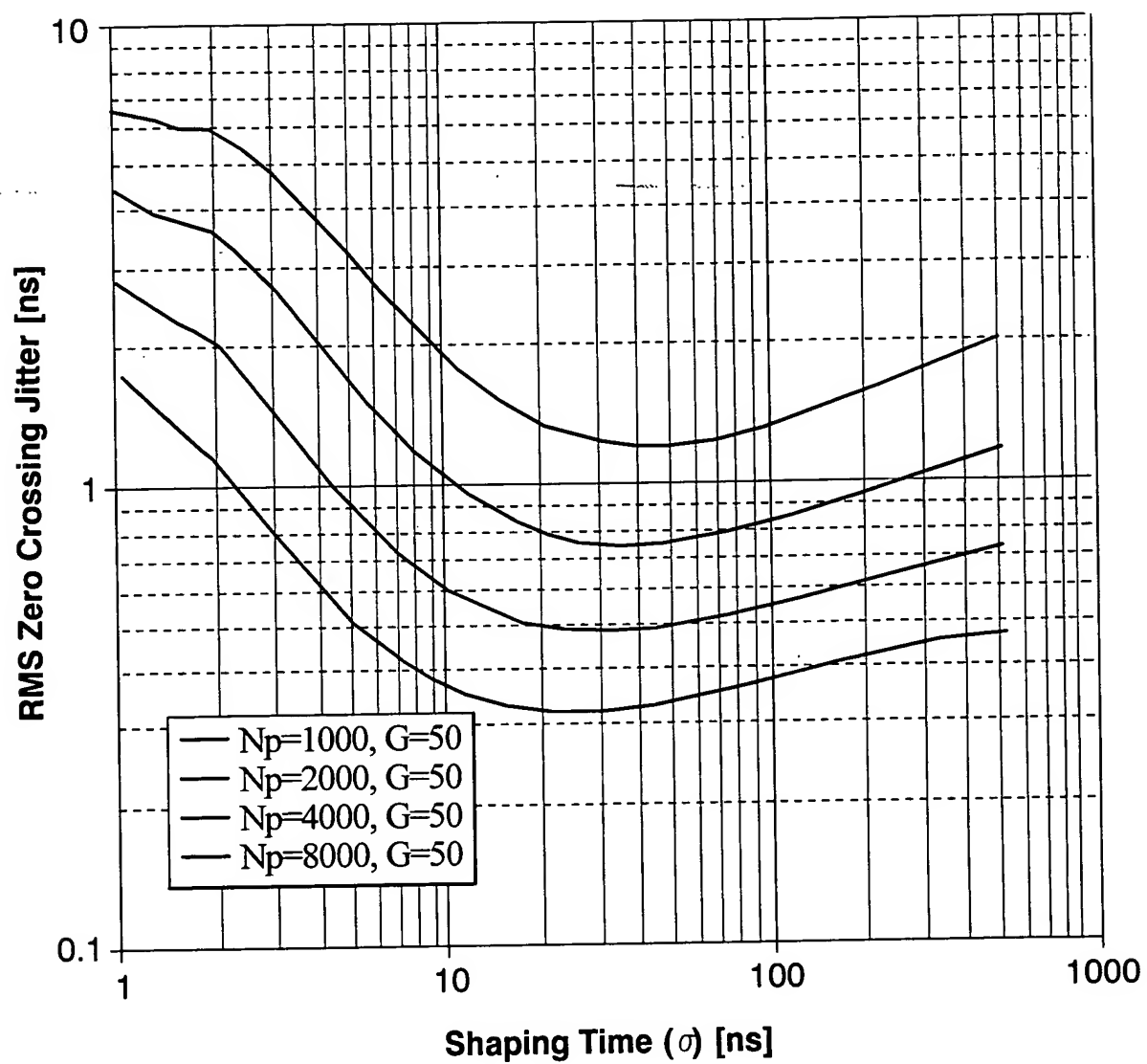
**Figure 25**



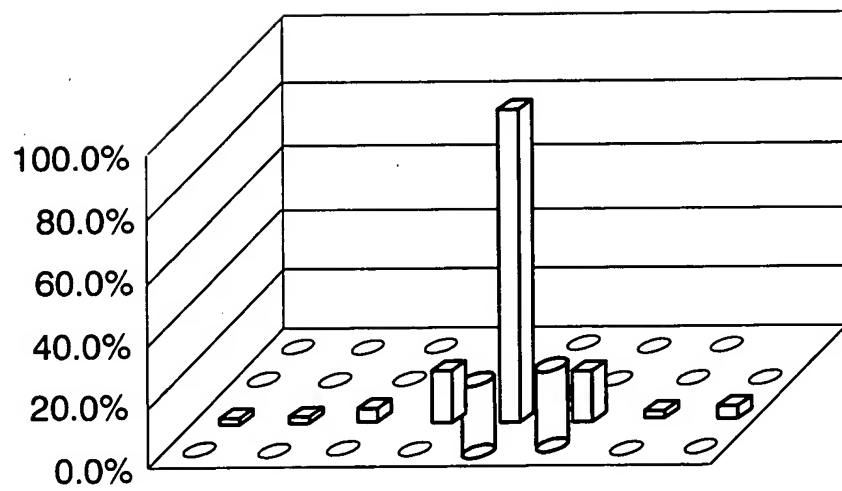
**Figure 26**



**Figure 26a**



**Figure 27**



**Figure 28**